Organic Electronics 13 (2012) 778–783

Contents lists available at SciVerse ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

Letter

Solution-processed low leakage organic field-effect transistors with self-pattern registration based on patterned dielectric barrier

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ARTICLE INFO

Article history:
Received 12 December 2011
Received in revised form 1 February 2012
Accepted 4 February 2012
Available online 17 February 2012

Keywords:
Organic field-effect transistor
Patterned dielectric barrier
Solution-processed
Leakage reduction
Selective wettability

ABSTRACT

We demonstrated a new type of a solution-processed organic field-effect transistor (OFET) in a bottom-gate, top-contact geometry where low leakage current and self-pattern registration were achieved using a patterned dielectric barrier (PDB). The PDB of a hydrophobic fluorinated-polymer was produced on the top of a polymeric gate insulator of poly(4-vinylphenyl) by transfer-printing. The PDB enables to effectively screen out the vertical charge flow generated from the gate electrode, and thus the vertical leakage current between the gate and the drain was reduced by two orders of the magnitude compared to the leakage current in a conventional OFET without the PDB. Moreover, the PDB defines spontaneously an active channel pattern from a solution of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS PEN) by means of the selective wettability and the geometrical confinement.

Solution-processed organic field-effect transistors (OFETs) have great potential for use in future flexible electronics because of large-area, low-cost, and low temperature processing capabilities [1–3]. In the past decade, much effort has been made in developing a variety of organic semiconducting materials, devising new OFET device structures, and modifying organic–organic and organic–metal interfacial interactions [4–7]. Recently, the electrical properties of the OFET have been comparable to those of an amorphous silicon-based FET at a performance level for microelectronic applications.

Nevertheless, for most of the solution-processed organic devices, substantial amount of the leakage current remains as one of the detrimental problems. Such large leakage current inevitably causes the low on–off current ratio and deteriorates the device stability during operation [8]. It is expected that in addition to a gate insulator material itself, the subtle changes including the surface morphology [9,10], impurities [11], and the physico-chemical interactions [12,13] of the dielectric layer interfaced with an active semiconducting layer will strongly influence the magnitude of the leakage current. For conventional OFETs fabricated by vacuum deposition, the leakage current can be reduced by introducing an extra buffer layer of either a hybrid layer [14] or a self-assembled monolayer (SAM) [15] onto a gate insulator as shown in Fig. 1(a). A new type of a dielectric material, for example, an ultrathin cross-linked blend [16], can be also used as a gate insulator. However, for solution-processed OFETs, it has been a serious challenge to reduce the leakage current since different solvents for successive solution processes may alter the intrinsic physical and/or chemical properties of individual layers in the OTFTs. In other words, a proper selection of mutually inert materials and solvents is an important issue on the preservation of different functional layers during the subsequent solution process. Another issue is how to precisely pattern a soluble organic semiconductor (OSC) in channel regions for eliminating the crosstalk between neighboring OFET elements in an array.

For soluble OSCs, direct patterning such as inkjet printing [17] or transfer printing [18] is commonly utilized owing to the simplicity of processing while indirect patterning through physical delamination [19], self-organization on the SAMs [20–22], or the formation of bank structures [23,24] is often used for achieving high resolution and/or

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doi:10.1016/j.orgel.2012.02.003

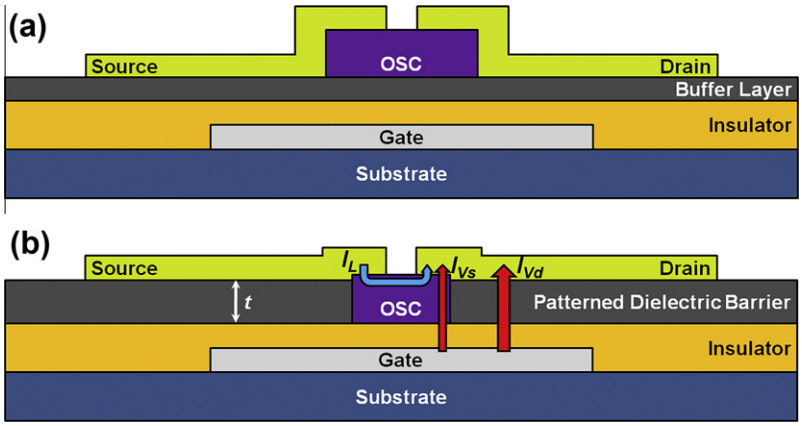

Fig. 1. The schematic illustration of (a) a typical bottom-gate, top-contact OFET structure with an extra buffer layer on a gate insulator for either the mobility enhancement or the leakage current reduction and (b) a new OFET structure with the PDB for self-pattern registration and low leakage current. The blue arrow and the two red arrows indicate the lateral current (I_L) and two contributions to the vertical current (I_{Vs} across the MISM region and I_{Vd} across the MIM structure), respectively. The thickness of the PDB is denoted by t. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

pattern generation. In fact, patterned OSC layers on a gate insulator enable to prevent undesired current pathways and result in the reduction of the off-current without sacrificing the mobility. Therefore, it is extremely important to develop a new OFET architecture suitable for solution-processing of the OSC and the gate insulator from the viewpoints of both the feature resolution and the chemical compatibility.

In this work, we introduce a novel concept, based on a patterned dielectric barrier (PDB) between the gate insulator and the source electrode as well as the drain electrode, to simultaneously achieve the reduction of the leakage current and the self-pattern registration of solution-processed OFETs in a bottom-gate, top-contact geometry as shown in Fig. 1(b). The PDB of a hydrophobic fluorinated-polymer was prepared on a gate insulator by transfer printing with a prescribed elastomeric stamp. The PDB leaves a cavity resembling a via-hole structure for an active region to facilitate self-pattern registration of a solution-processed OSC. In this PDB configuration, as the PDB thickness increases, the vertical charge flow between the gate and the drain becomes essentially screened out, meaning that the vertical current is tremendously reduced. Moreover, the selective wetting properties of the PDB allow to spontaneously pattern a solution of the OSC into the cavity like a via-hole structure.

In general, the leakage current in an OFET has two physical origins, one of which is the lateral current (I_L) along the OSC layer from the source electrode to the drain electrode and the other is the vertical current across the gate insulator from the gate electrode to the drain electrode. More specifically, the vertical current consists of the current (I_{Vs}) across a metal–insulator–semiconductor–metal (MISM) region and the current (I_{Vd}) across a metal–insulator–metal (MIM) region as shown in Fig. 1(b). Note that the latter is the major contribution to the leakage current, and it depends strongly on the dielectric properties of the PDB. In contrast to Fig. 1(a) where a gate insulator is entirely covered with an extra buffer layer, the OSC in Fig. 1(b) is in direct contact with a gate insulator. Thus, the magnitude of the lateral current remains essentially unchanged irrespective of the PDB.

The fabrication processes for the OFET with the PDB and the microscopic image of the fabricated OFET are shown in Fig. 2(a) and (b), respectively. The elastomeric stamp having desired patterns of the dielectric barrier, complementary to the OSC patterns, was made of poly(dimethylsiloxane) (PDMS) (Sylgard 184, Dow Corning). As shown in Fig. 2(a), the receiving substrate had a gate electrode (aluminum: Al) of 60 nm thick on which a gate insulator, poly(4-vinylphenol) (PVP) mixed with methylated poly(melamine-co-formaldehyde) (MMF) (100 wt.% of PVP) in propylene glycol methyl ether acetate (PGMEA) in 5 wt.%, was coated at the spinning rate of 3000 rpm for 30 s, followed by the subsequent thermal cross-linking at 200 °C for 30 min. The gate insulator was 100 nm thick. For the PDB, a hydrophobic fluorinated-polymer (Novec™ EGC-1700, 3M) dissolved in a fluorinated-solvent (Novec™ HFE-7100, 3M) was transfer-printed onto the substrate using the PDMS stamp with complementary patterns of the OSC. Due to the low surface energy of the PDMS compared to that of the underlying gate insulator, the PDB on the PDMS stamp was easily transferred without any additional treatment such as pressure and/or heat [25]. The OSC used in this study was 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS PEN) of 1 wt.% dissolved in anisole. It should be noted that the solvent (anisole) is chemically inert to both the fluorinated-polymer PDB and the PVP insulator. As clearly seen in Fig. 2(b), the TIPS PEN droplet was spontaneously confined only in the cavity formed by the PDB through selective wetting. The TIPS PEN was thermally baked at 60 °C for 30 min. The source and drain electrodes were then prepared onto the TIPS PEN film by thermal evaporation of gold (Au) through a metal shadow mask to define a channel with the length of 50 μm and the width of 1000 μm. In Fig. 2(b), the MISM region (6.1×10^{-3} cm^2) was enclosed by white dashed lines and the MIM region (5.0×10^{-3} cm^2) by black dashed lines. These regions represent the overlap areas

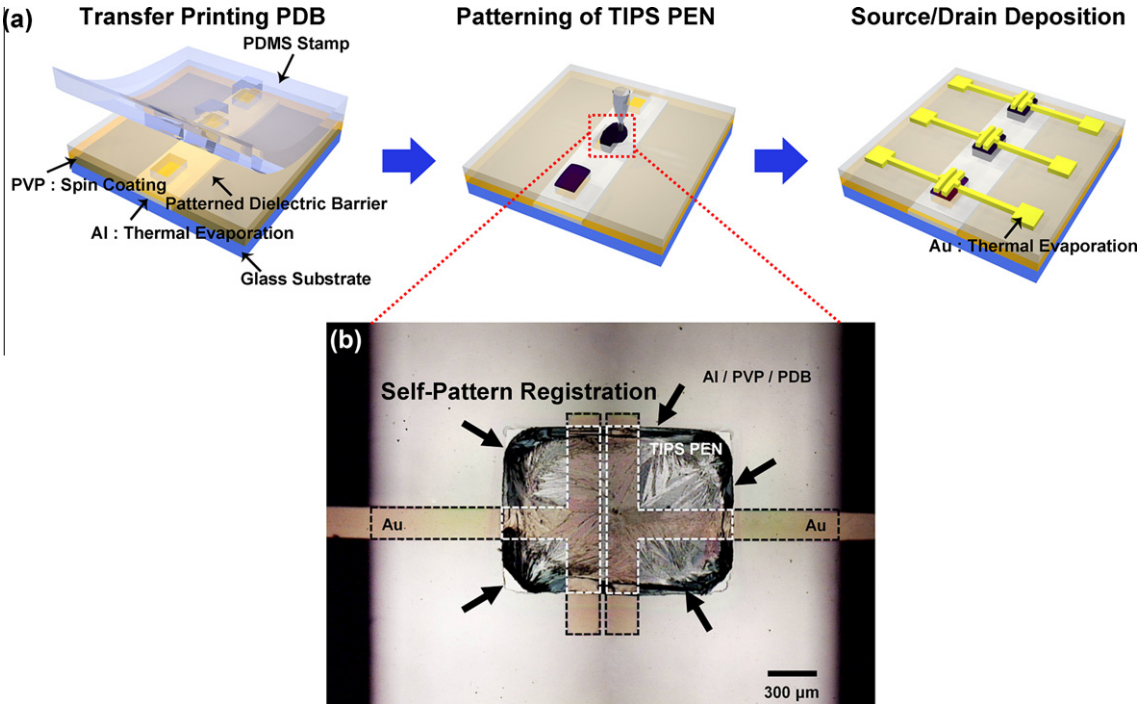

Fig. 2. (a) The fabrication processes for the OFET with the PDB. (b) The microscopic image of the top-view of the fabricated OFET. The MIM and MISM regions were enclosed by black dashed lines and white dashed lines, respectively. The black arrows represent the pattern boundary of self-registration.

between two top (source and drain) electrodes and the bottom (gate) electrode in our OFET structure.

Let us first describe the current characteristics of the MISM structure and two MIM structures (one of which having only a gate insulator and the other having a fluorinated-polymer layer on a gate insulator) to investigate how the PDB affects the leakage current in the OFET. Fig. 3(a) shows the current density in the MISM capacitor (Al/PVP/TIPS PEN/Au) as a function of the applied voltage. The voltage applied to the Al electrode was swept from −5 V to 5 V while the Au electrode was grounded. The measured current density was less than 10^{-6} A/cm^2 in the range of the applied voltage up to 5 V, which contributes to the vertical current in the OFET. Note that the magnitude is much smaller than the leakage current observed in typical OFETs [14,15,26], indicating that the current flow across the MISM region in the channel of the OFET is not the major contribution to the leakage current. The asymmetry in the leakage current with respect to zero applied voltage in Fig. 3(a) is attributed to the p-type nature of the TIPS PEN. As shown in Fig. 3(b), the MIM with only the PVP layer of 100 nm thick as a gate insulator exhibited the current density of about 10^{-3} A/cm^2 at the applied voltage of 5 V while the MIM with an additional fluorinated-polymer PDB of 200 nm thick on the PVP layer showed the current density of about 10^{-9} A/cm^2 at the same applied voltage. In other words, the current density in the MIM structure was reduced by six orders of the magnitude by the introduction of a fluorinated-polymer layer as a dielectric barrier. Note that the symmetry in the leakage current with respect to zero applied voltage was fully preserved.

Based on the above results, we now examine the role of the PDB on the current characteristics of our OFET shown in Fig. 1(b). Two contributions to the leakage current depending on the current flow direction were independently measured as a function of the thickness (t) of the PDB. The PDB thickness was varied with the dip-coating rate and the concentration of the fluorinated-polymer solution.

Fig. 3(c) shows the lateral current measured at −5 V for the drain voltage and 0 V for the source and gate voltages together with the vertical current at −5 V for the gate voltage and 0 V for the source and drain voltages among three electrodes. Note that in our case, under the conditions that both the source and gate voltages are zero, the current flowing from the source to the drain through the OSC, not passing via the gate electrode, corresponds to the lateral current. The vertical current decreases rapidly with increasing the PDB thickness, supporting that the PDB is indeed capable of screening out the vertical charge flow across the dielectric layer of the PVP between the source (or drain) electrode and the gate electrode, namely, in the MIM region. In contrast, the lateral current between the source electrode and the drain electrode remains fairly constant. The vertical current decays and eventually reaches a certain background value as the PDB thickness increases. As shown in the inset of Fig. 3(c), the decay behavior of the vertical current is analyzed in a form of $I_V = I_{V0} + I_{V1}\exp(-t/l)$ where I_{V0} denotes the background value and I_{V1} represents the decaying part of the vertical current with the characteristic length l for the charge screening process. In fact, I_{V0} corresponds to the vertical current in the MISM and the characteristic length l

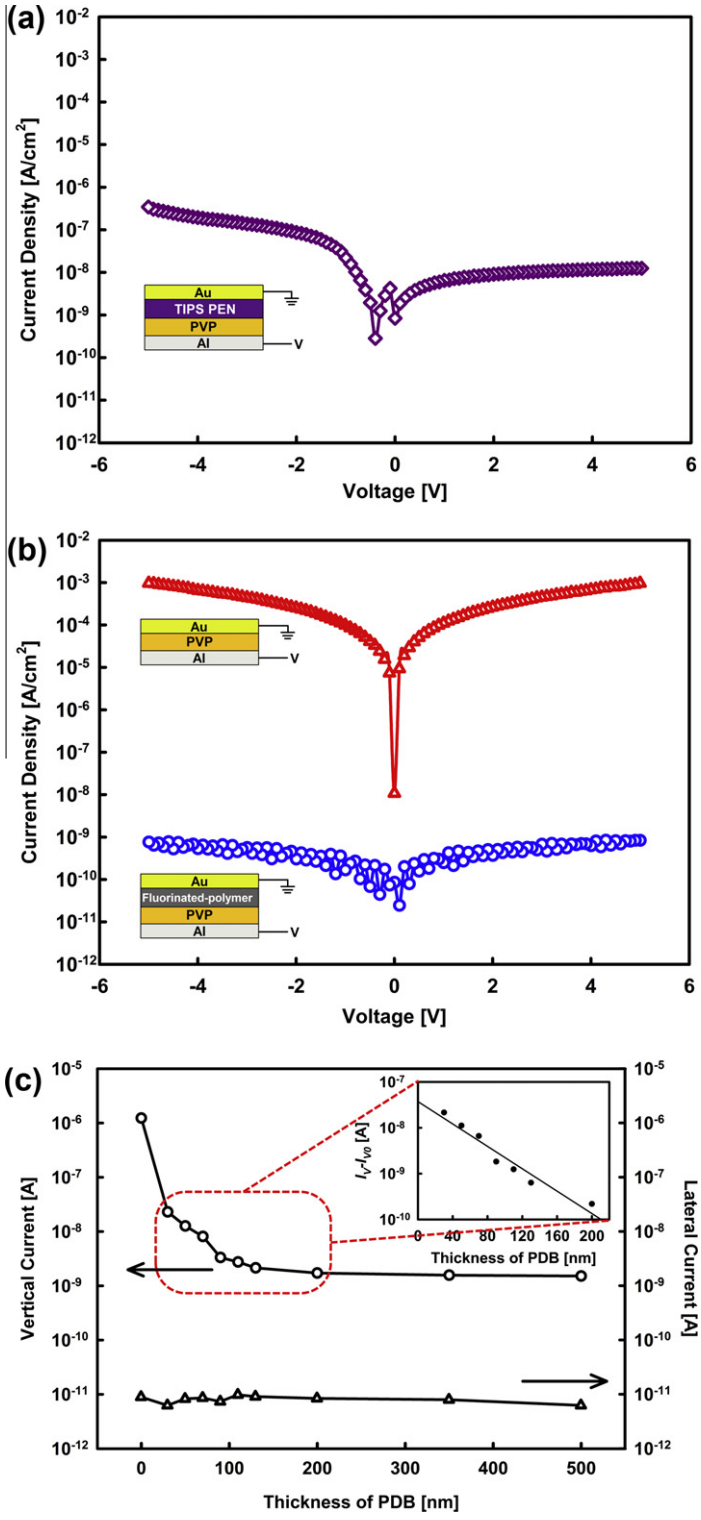

Fig. 3. (a) The current density in the MISM capacitor of Al/PVP/TIPS PEN/Au as a function of the applied voltage to the Al electrode. (b) The current densities in two MIM capacitors of Al/PVP/Au and Al/PVP/fluorinated-polymer/Au as a function of the applied voltage. Open red triangles and open blue circles represent the current density of Al/PVP/Au and that of Al/PVP/fluorinated-polymer/Au, respectively. (c) The vertical current (open circles) and the lateral current (open triangles) in our OFET as a function of the thickness of the PDB. The inset shows the semi-logarithmic plot of $(I_V - I_{V0})$ as a function of t below 200 nm. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

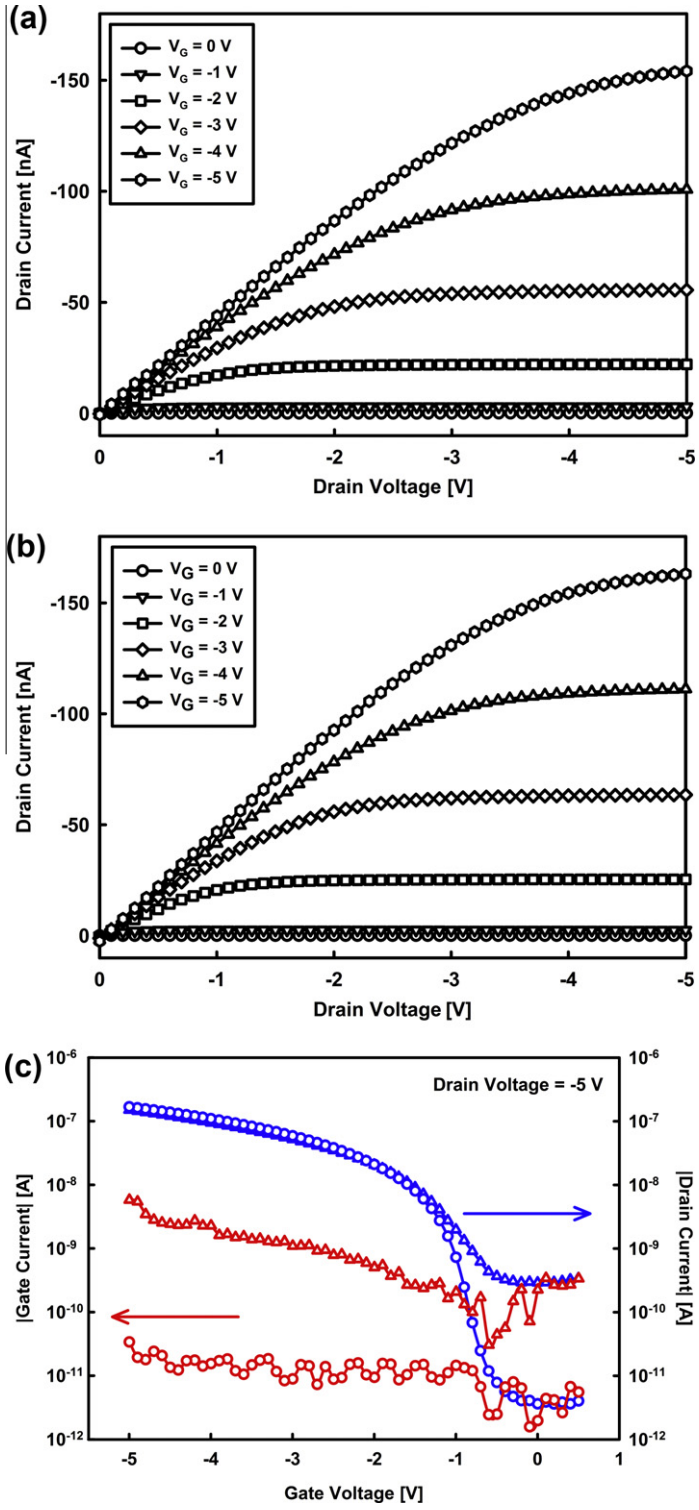

Fig. 4. The output characteristics measured with varying the gate voltage from 0 V to −5 V in a step of −1 V for (a) the OFET without the PDB and (b) the OFET with the PDB (t = 200 nm). (c) The drain current and the gate current at the drain voltage of −5 V as a function of gate voltage. Blue and red symbols represent the drain current and the gate current, respectively. Open circles and open triangles correspond to the OFET with the PDB and the OFET without the PDB, respectively. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

depends on the material parameters as well as the interfacial properties of the PDB. Fitting the experimental data to the above form of the vertical current with the help of $I_{V0} = 1.50 \times 10^{-9}$ A taken at t = 500 nm where the vertical

current vanishes in the MIM but remains in only the MISM, we have $I_{V1} = 3.73 \times 10^{-8}$ A and $l = 35.7$ nm. Converting the current density measured in the MISM at the voltage of −5 V in Fig. 3(a) into the leakage current by the multiplication of the effective MISM area (6.1×10^{-3} cm^2) enclosed by white dashed lines in Fig. 2(b), the vertical current I_{Vs} was estimated to be 2.10×10^{-9} A. Note that this value of I_{Vs} is exactly on the same order of the magnitude of I_{V0}. Taking into account the variations of the thickness and the interfacial properties of the TIPS PEN between the two cases, the OFET in Fig. 2(b) and the MISM capacitor in Fig. 3(a), it is physically reasonable to claim that I_{Vs} is represented by I_{V0}.

The electrical properties of our OFETs with the PDB were measured as a function of the applied voltage using a semiconductor parameter analyzer (HP 4155A, Agilent Technologies). The output characteristics of the OFETs without and with the PDB of 200 nm thick, measured with varying the gate voltage from 0 V to −5 V in a step of −1 V, are shown in Fig. 4(a) and (b), respectively. Clearly, in both types of the OFETs, a very well-defined saturation behavior of the drain current was obtained as a function of the drain voltage. Basically, no difference in the output characteristics between the two types of the OFETS was observed regardless of the presence of the PDB. This tells us that the PDB does not influence the lateral charge transport along the TIPS PEN layer in contact with the PVP insulator.

Fig. 4(c) shows both the drain current and the gate current for two types of the OFETs, one of which having no PDB and the other having the PDB of 200 nm thick, at the drain voltage of −5 V as a function of gate voltage. As shown in Fig. 4(c), extremely low gate current (<10 pA) was obtained in the OFET with the PDB and it was two orders of the magnitude lower than the gate current in the OFET with no PDB. Moreover, the drain current on–off ratio was much increased from 5.2×10^2 to 4.7×10^4 in the low operation voltage regime. For both OFETs, the field-effect mobility in the saturation region, $(3.5 \pm 0.3) \times 10^{-2}$ cm^2/V s, was found to be nearly identical and the threshold voltage was about −0.5 V.

In summary, we demonstrated a novel architecture of the OFET where the PDB was introduced to simultaneously achieve the leakage current reduction and the self-pattern registration of the soluble OSC. The leakage current was reduced by two orders of the magnitude compared to that for a typical OFET with no PDB. The physical origin of the leakage current in the OFET was systematically analyzed in terms of the lateral and vertical contributions, one of which corresponds to the current flow along the OSC layer and the other to the current flow across the MIM as well as the MISM. The PDB is capable of effectively screening out the vertical charge flow and providing a cavity like a via-hole structure. Finally, our approach presented here would provide a basis for developing solution-processed integrated circuits that have low current leakage current and small operation voltages.

Acknowledgment

This work was supported by the National Research Foundation of Korea under the Ministry of Education, Science and Technology of Korea through the Grant No. 2011-0028422.

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